Amendments to the Drawings:

None

REMARKS/ARGUMENTS

Claims 11, 14, and 19-22 stand rejected under 35 U.S.C. 102(b) as being anticipated by Hsu; claims 12 and 13 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu in view of Lin.

Claim 11 comprises the limitations of forming at least a first and second active regions in said well region by forming a contact isolation structure in said well region between said first isolation region and said second isolation region, forming a gate dielectric layer on said first active region and said second active region, and forming a gate layer on said gate dielectric layer wherein said gate layer overlies said first active region, said second active region, and said contact isolation region. The Hsu patent in Figure 2 forms first and second active regions by forming the isolation structure 34. The subsequent gate structure 46 in the Hsu patent extends only over one of the active regions formed in Figure 2. From Figure 7 this would be the active region formed to the left of the isolation structure 34. Claim 11 requires the gate layer (46 in the Hsu patent) to overlie said first active region, said second active region, and said contact isolation region. This is not shown in the Hsu patent and claim 11 is allowable over the Hsu patent under 102(b). Furthermore, claims 12-14 depend on claim 11 and therefore contain all the limitations of claim 11. The Lin patent does not contain the feature described above and claims 12-14 are therefore also allowable over the Hsu patent either singly or in combination with the Lin patent.

Claim 19 comprises the limitations of forming a well region of a first conductivity type in a semiconductor substrate; forming a gate dielectric layer on said well region; forming a gate layer on said gate dielectric layer; forming contact regions in said well region of a first conductivity type wherein said contact regions are formed using a source and drain region implantation formation process; and forming gate layer contacts to said gate conductive layer wherein said gate layer contacts overlie an isolation region. The examiner is directed to the limitations of the contacts to the well region being of the same conductivity type as the well region. The Hsu patent teaches in col. 4,

lines 41-46 that the source and drain regions 60, 62 are of opposite conductivity type to the well region 63. The well region 63 is p-type and the source and drain regions 60, 62 are n-type. Claim 19 is therefore allowable over the Hsu patent. Furthermore, claims 20-22 depend on claim 19 and therefore contain all the limitations of claim 11. Claims 20-22 are therefore also allowable over the cited art.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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